REMARKS

Below, the applicant's comments are preceded by related remarks of the examiner set forth in small bold type.

Claim 31 is objected to because of the following informalities: Claim 31 is dependent upon claim 4. However, claim 4 and those claims upon which claim 4 is dependent upon do not provide proper antecedent basis for "the filtered voltage signal". Therefore, since claim 30 would provide proper antecedent basis it is assumed for examining purposes that a mere typo in the dependency of claim 31 has occurred and that the actual dependency of claim 31 is that of claim 30 and not claim 4. Appropriate correction is required.

Claim 31 has been amended to depend on claim 30.

Claim 1 is rejected under 35 USC 102(b) as anticipated by Clarke 6,337,604 (Clarke) or, in the alternative, under 35 USC 103(a) as obvious over Clarke 6,337,604 (Clarke) in view of Ochiai et al. US 4,851,792 (Ochiai).

The single Figure of Clarke discloses a circuitry for controlling the oscillating frequency of an oscillator (See column 2, line 22), the circuitry having a plurality of on-chip capacitors C1-C6 (Note that the capacitors are part of the "integrated circuit" 3 and thus are on-chip capacitors), each of which is independently selectable by a control signal D0-D5, and each of which provides a controllable amount of capacitance to the oscillator to control the oscillating frequency of the oscillator (See column 2, line 22). Claim 1 has been previously amended to recite a bias circuit to provide a substantially constant voltage to the bias at least one of the plurality of capacitors. As noted in the remarks below the examiner cannot find a reference in the original specification or disclosure to a "substantially constant voltage" as is relates to the bias voltage applied to the capacitors. Therefore, V_{bias} and V_{cc} that is considered to be a bias voltage for the capacitors in Clarke are considered to be a "substantially constant voltage". (Note that changes in V_{bias} would cause changes in the oscillator, i.e. the operating point of transistors Q1, Q3, Q4 and Q5 would change, which logically is incorrect for the typical operation of an oscillator.)

However, alternatively Figure 8(a) discloses a biasing arrangement for the capacitors of an oscillator and is configured such that the bias voltage VB of the capacitor 14 "remains constant". This as recognized by Ochiai allows for the oscillation frequency to remain constant (See column 5, around line 61).

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the oscillator arrangement of Clarke with a bias arrangement that keeps the necessary bias voltage of the capacitor elements constant so as to prevent drift in oscillator frequency as taught by Ochiai.

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Claims 3-6 and 33 recite conventional forms of capacitors that make up the frequency changing capacitors of the oscillator. Clarke is silent on these.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted any of the conventional capacitors as recited by the claims of the instant application in place of the generic capacitors of Clarke because, as the reference is silent as to the exact composition of the capacitors one of ordinary skill in the art would have been motivated to use any art-recognized equivalent capacitors such as the well-known capacitors as recited by the claims of the instant application.

Page 6, lines 18-21, and FIG. 2 of the applicant's specification provides an example of a "substantially constant voltage" that biases at least one MOSFET capacitor, as recited in claim 1. The specification describes a V_{CC_FILTER} signal derived from the power supply signal V_{CC} to bias the PMOS capacitors into saturation; most of the high frequency noise contained in the V_{CC} signal is filtered by a low pass filter.

Neither Clarke nor Ochiai discloses or suggests "drain-source connected MOSFET capacitors, each of which is independently selectable by a control signal, and each of which provides a controllable amount of capacitance to an oscillator to control an oscillating frequency of the oscillator," as recited in amended claim 1.

Although Clarke discloses a bank of load capacitors C1 to C6 (see figure), Clarke is silent on the type of capacitor to be used for C1 to C6. Although Ochiai discloses the use of a floating gate MOS variable capacitor (col. 4:8), Ochiai does not disclose or suggest the use of drain-source connected MOSFET capacitors.

It would not have been obvious to use drain-source connected MOSFET capacitors to provide controllable amounts of capacitances to an oscillator to control the oscillating frequency of the oscillator. Without proper design, the capacitances of the MOSFET capacitors may vary with changes in the power supply voltage, and there may be leakage current from source or drain nodes to the body of a MOSFET, causing the capacitance to change, which in turn causes the oscillating frequency to change. The applicant requests that the examiner provide a reference that discloses use of drain-source connected MOSFET capacitors that are coupled to an oscillator to control the oscillating frequency of the oscillator.

Claims 2-4, 7-12, and 30-35 are patentable for at least the same reasons as claim 1.

Claims 13, 15, 16 and 24-29 are rejected under 35 U. S. C. 103(a) as being unpatentable over Horn "Basic Electronics Theory" 4th Edition pp 377-378 and pp 454-465 in view of Clarke US 6,337,604 (Clarke).

Beginning on page 420 of Horn, Horn describes the basic well-known structure of a computer. Horn describes the speed of the computer that as known by those of ordinary skill this is describing the oscillator or "real time clock" that is inherently within the computer. Also within a computer, computers inherently have a system time signal that represents at least one of hour, minute and second and this is the clock signal itself. For example 100 clock pulses will represent X number of seconds, etc.. Note that software will take this will take this and display on a monitor the hours, minutes and seconds of a day but the claims only requires a system time signal that represents at last one of hour, minute and second. Horn is silent on the specifics of the oscillator or real time clock or just clock.

The single Figure of Clarke discloses a circuitry for controlling the oscillating frequency of an oscillator (See column 2, line 22), the circuitry having a plurality of on-chip capacitors C1-C6, each of which is independently selectable by a control signal DO-D5, and each of which provides a controllable amount of capacitance to the oscillator to control the oscillating frequency of the oscillator (See column 2, line 22).

The single Figure of Clarke also discloses an electronic device comprising a real time clock, i.e. oscillator, for generating a system time signal "CLK OUT 5 " (See the only Figure and column 2, around line 20), the real time clock having a digitally tunable oscillator (Note the use of set of shift registers 21) for digitally adjusting an operating frequency of the real time clock to speed up or slow down the system time signal (See column 3, lines 45), and a memory device 21 for storing data representing a configuration of the digitally adjusted tunable oscillator.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the conventional real time clock/oscillator circuit of Clarke for the oscillator/real time clock/clock of Horn because, as the reference is silent as the exact oscillator/clock circuit employed one of ordinary skill in the art would have been motivated to use any art-recognized equivalent switch such as the well-known, conventional oscillator/clock circuit of Clarke.

The applicant disagrees. Horn does not disclose or suggest a circuit "to generate digital control signals to control the digitally tunable oscillator to adjust the operating frequency of the real time clock to speed up or slow down the system time signal," as recited in amended claim 13.

What Horn describes is increasing the frequency of a system clock oscillator to increase the operating speed of a computer (page 425), not adjusting the frequency of a real time clock to speed up or slow down the system time signal. The system time signal and the real time clock are different in the applicant's claim 13. For example, a computer system clock (which governs CPU

operations) may operate at 1GHz, while its real time clock operates at 32,768 Hz. A faster computer may have a faster system clock, such as at 2 GHz, but the real time clock may still operate at 32,768 Hz. Horn's description of increasing the system clock to increase computer operating speed has nothing to do with adjustment of the real time clock to speed up or slow down the system time signal.

What is lacking in Horn is also not disclosed or suggested in Clarke, which merely describes a "standard CMOS clock signal" (col. 2:20) whose frequency can be adjusted by using control lines D0 to D5 to select different capacitors C1 to C6. Clarke does not disclose or suggest generating digital control signals to control a digitally tunable oscillator to adjust the operating frequency of the real time clock to speed up or slow down the system time signal.

Claims 16 and 24 are patentable for similar reasons as claim 13. Claims 6, 14, 15, 17, 18, 25-29 are patentable at least for the same reasons as the claims on which they depend.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance that the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Please apply $140 for excess claims fee and any other charges to deposit account 06-1050, referencing attorney docket 10559-650001.

Respectfully submitted,

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** See attached document certifying that Rex Huang has limited recognition to practice before the U.S. Patent and Trademark Office under 37 CFR § 10.9(b).*

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Expires: January 1, 2005

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